What is claimed is:

1. A method for forming a wrap-around-gate field-effect transistor on a handle wafer, comprising the steps of:

forming a silicon-on-insulator (SOI) structure on the handle wafer, the SOI structure comprising a silicon island between a first oxide layer and a second oxide layer;

creating a first cavity in the SOI structure extending from a top surface of the SOI structure to the handle wafer, the first cavity having substantially vertical sidewalls and intersecting the silicon island;

isotropically etching the first oxide layer and the second oxide layer within the cavity thereby exposing surface portions of the silicon island;

depositing on the surface portions a gate conductor material; and

isotropically etching the gate conductor material to form a wrap-around gate electrode circumscribing a periphery of the silicon island.

2. The method of claim 1, further comprising the step of:

forming a gate dielectric on the surface portions.

3. A method for forming a wrap-around-gate field-effect transistor, comprising the steps of:

creating a first cavity in an SOI structure that intersects a semiconductor island buried in oxide material;

etching the oxide material within the first cavity thereby exposing surface portions of the semiconductor island;

depositing on the surface portions a gate conductor material;

etching the gate conductor material to form a wrap-around gate electrode that encircles more than half of a periphery of the semiconductor island.

4. The method of claim 3, further comprising the step of:

forming a gate dielectric on the surface portions.

5. The method of claim 3, further comprising the step of:

forming an silicon-on-insulator (SOI) structure on a handle wafer.

6. The method of claim 3, wherein the first cavity includes substantially vertical sidewalls.

7. The method of claim 4, wherein the first cavity extends from a top surface of the SOI structure to the handle wafer.

8. The method according to claim 3, wherein the oxide material comprises a first oxide layer on the handle wafer below the semiconductor island and a second oxide layer above the semiconductor island.

9. The method of claim 8, further comprising the step of:

forming a hard mask on the second oxide layer, the hard mask including an aperture defining the first cavity.

10. The method of claim 9, wherein the step of etching the first and second oxide layers is performed anisotropically, using an aperture in the hard mask.

11. The method of claim 8, wherein the step of depositing further includes the steps of:

forming gate dielectric material on the surface portions;

depositing a conformal gate conductor material layer within the first cavity to cover exposed portions of the first and second oxide layers and the silicon island; and

depositing an organic fill material to fill the first cavity.

12. The method of claim 11, further comprising the step of:

after depositing the organic fill material, directionally etching a second cavity based on an aperture in the hard mask until at least a portion of the gate conductor material is exposed within the second cavity.

13. The method of claim 12, wherein the second cavity includes substantially vertical sidewalls.

14. The method of claim 12, further comprising the step of:
stripping the organic fill material from the second cavity.

15. The method of claim 9, further comprising the step of removing the hardmask.

16. The method according to claim 8, further comprising the step of:
removing the first and second oxide layers.

17. The method according to claim 3, further comprising the steps of:
forming source/drain regions on the semiconductor island; and
forming a first contact connected to the gate conductor material and a second contact connected to the source/drain regions.

18. The method according to claim 3, further comprising the step of:
controlling a gate length of the wrap-around-gate field-effect-transistor by controlling the etching of the oxide material and the gate conductor material.

19. The method according to claim 18, wherein the step of controlling includes the steps of:
anisotropically etching the oxide material a first distance from a vertical edge of the first cavity;
isotropically etching the gate conductor material a second distance from the vertical edge of the first cavity, the second distance being less than the first distance; and
wherein the gate length is substantially the difference between the first distance and the second distance.

20. A portion of a wrap-around-gated field-effect transistor, the portion comprising:

an silicon-on-insulator (SOI) island comprising side surfaces forming a periphery and extending, for a length, along a major axis in the horizontal direction; and

a gate electrode surrounding and supporting the SOI island, the gate electrode extending in a vertical direction from a handle wafer and having a thickness, in the horizontal direction, less than the length of the SOI island such that a portion of the SOI island extends on one side of the gate electrode and another portion of the SOI island extends on another side of the gate electrode, the gate electrode comprising:

a first portion below the SOI island, a second portion on one side of the SOI island, and a third portion above the SOI island such that the gate electrode extends more than half-way around the periphery of the SOI island.

21. The portion according to claim 20, wherein a first edge face of the SOI island extends outward on one side of the gate electrode and a second edge face of the SOI island extends oppositely outward on another side of the gate electrode.

22. The portion according to claim 20, wherein the gate electrode has a cross-sectional profile that is C-shaped.

23. The portion according to claim 20, wherein a portion of a top surface of the SOI island is exposed.

24. The portion according to claim 20, wherein at least a portion of the SOI island is supported underneath by an oxide layer on the handle wafer.

25. A field-effect-transistor comprising:

a silicon-on-insulator (SOI) island comprising a surface periphery and two edge faces, the SOI island oriented substantially in a horizontal direction;

a wrap-around gate electrode oriented in substantially a vertical direction intersecting with the SOI island in-between the two edge faces such that the SOI island, such that the wrap-around gate electrode extends more than half-way around the surface periphery of the SOI island;

a source region formed on a first part of the SOI island, on one side of the gate electrode; and

a drain region formed on a second part of the SOI island, on another side of the gate electrode.

26. The field-effect transistor of claim 25, wherein a portion of a bottom surface of the SOI island on both sides of the gate electrode is exposed.

27. The field-effect transistor of claim 25, wherein at least a portion of the SOI island is supported underneath by an oxide layer.

28. The field-effect transistor of claim 25, wherein the wrap-around gate electrode extends entirely around the surface periphery of the SOI island.